Power Reduction with FlipFlop Grouping in Data Driven Clock Gating

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***Abstract*—**In digital circuits Clock signal is one of the factor causing dynamic power consumption.Clock Gating is a method applied for reducing the dynamic power dissipation in sequential circuits.Here the redundant clock pulses in a high frequency clock signal are eliminated by performing AND operation on Enable signal and applied clock signal.Enable signal is determined by performing XOR operation on input and output of sequential element such as Flipflop.ANDed output—the Gated clock signal serves as clock to the existing circuit, which consists of clock pulses at the switching activities of input signal.This method can be extended to group of Flipflops having similarly switching inputs by performing OR operation on the enable signals of all Flipflops in the group.When this group drives a combinational circuit the leakage power exists,when the circuit is in stand-by mode i.e no existence of pulse in Gated clock signal.For eliminating this,we are introducing Power gating in which Gated clock signal is given as a sleep signal to NMOS transistor in pull down section.The simulation results are carried out on Tanner EDA tool.The simulation shows that the design has more efficient with less power consumption in CMOS techniques.

Keywords—*ClockGating,Gatedclocksignal,PowerGating,Tanner EDA tools*

I. INTRODUCTION

The dynamic power consumption in the digital circuits mainly depends on the supply voltage V_{dd},output capacitance and frequency of the clock signal.Among them clock frequency is the major consumer,because normally the clock signal is of high frequency[1].Clock gating is applied system,logic and gate levels[2],[3].Clock gating serves the dynamic power reduction by eliminating the redundant clock pulses with the help of enable signal.In the earlier days the enable signal is supplied manually by synthesizing the input of functional element.This enable signal comprises of clock pulses at the switching time instants of input signal.Both enable and actual clock are given as inputs to the logical AND gate,the obtained output is now the clock for the existing functional element as shown in Fig1.These can be better described in[4] –[6]

The method of determining the enable signal by synthesizing input is flexible with one or two functional elements but causes the complexity with group of functional elements.Also,manual determination of enable signal is a time consuming process.So,there is a need of tracing a new method of generating clock enable signal automatically to a group of elements.For this we are going to incorporate modules of logic gates.The module consists of XOR gates and OR gates.The usage explained in section II.

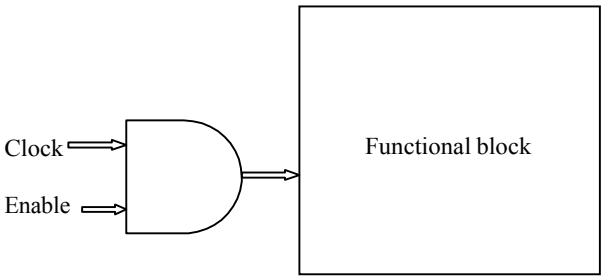

FIG 1 SIMPLE CLOCKGATING

The data-driven elements are also subjected to clock gating to avoid redundancy in terms of dynamic power dissipation.The switching in data either from 0-1 or 1-0 states is taking as the constraint for applying the gating.Whenever there no occurrence of new data the clock is gated to the flipflop and the same is happen to group of such flipflops[7].The large number of flipflops driven by same clock signal are subjected to clock gating by grouping.

Multi-bit flipflop gouping is the existed grouping of flipflops for reducing the number of inverters driving the slave latch and the corresponding power wastage[9]and[10]. Unfortunately this cannot be applied to large number,because it depeds on physical proximity of flipflops.This can be efficient for two or three in number ,which is also known as sharing of inverters.The inverter driving the slave latch is shared with latches of other flipflops.In the recent years grouping is done based of toggling similarity [8] and at the same time physical proximity which includes increased number of flipflops.The ouputs obtained from this group may be further processed by combinational circuits. To avoid the leakage power when the circuit is in stand-by mode we are going to include power gating within it.SectionII describes the automatic generation of clock enable signal.Grouping and optimized gated clock signal generation is discussed in sectionIII. How to include the power gating is discussed in sectionIV.

The obtained experimental results are listed in section V.Conclusion and future scope are explained in section VI.The described methods are applied to the below circuit fig 2 and compared for power consumption.

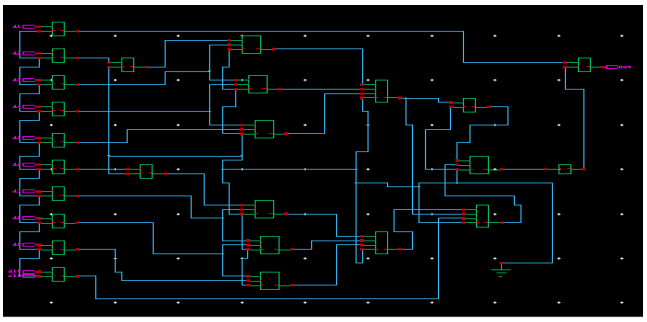

Fig 2 Normal circuit to which given method are applied

II. AUTOMATIC GENERATION OF CLOCK ENABLE SIGNAL

Generation of clock enable signals at gate level is better explained.The input data and ouput data of the flipflop is taken as the inputs for XOR gate,the output of the XOR gate will be the enable signal for that flipflop.From the truth table of XOR gate in table 1.

x	y	x XOR y
0	0	0
0	1	1
1	0	1
1	1	0

Table 1 XOR truth table.

By including the XOR gate in the circuit we can automatically generate enable signal as per the operation of XOR gate.For this the input and output signals of the flipflop are given as two inputs for the XOR gate,as per the truth table,when input and output of particular flipflop are same,the output will null and no enable signal is obtained when they are different enable signal is obtained.
*Case1:*If the logic 1 is input data of D-flipflop at a particular clock edge it is passed to output and remains until the occurrence of next clock edge.If there is no change in the next clock edge,the output remains same.If this situation exists for long period of time,the clock pulses in this period of time are redundant.These are blocked as per XOR gate operation.

*Case2:*If the input data has changed to logic 0 within short period of time,then 0 is XORed with preserved data logic 1 and then ouput will be logic 1,which indicates the generation of enable signal at the change of input data.This can be stored at output.
Fig 3 shows the integrated clock gating for a group of flipflops.Here the enable signal is generated for individually for all flipflops as explained above.The obtained enabled signals from all the flipflops are ORed with logical OR gate.The ouput of OR gate gives the combined enable signal of entire.This signal is ANDed with original clock signal. Before ANDing the output of OR gate is passed through latch for glitch-freed enable signal.The collective method of integrating all these modules is commercially termed as Integrated clock gating(ICG)[11].

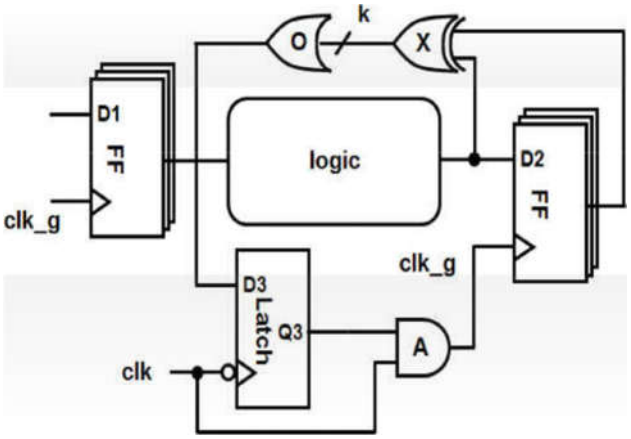

Fig 3 Integrated clock gating applied to group of flipflops

In the above circuit clk_g denotes the GATED CLOCK SIGNAL,which is the optimized clock signal for the entire group of flipflops.The clock pulses represented by the gated clock signal are desirable as in the switching of input data.
Thus the functional blocks or modules can be effectively capture the time periods when they need not be clocked.They can be synthesized at gate level for the automatic clock enable signal.By this less power is consumed by clock[14].

The outputs produced from the first group of flipflops are processed in the combinational circuit,which is represented as logic in the above fig 3.The processed data from the logic drives the flipflops in the next stage to which Integrated clock gating has been applied.

III. GROUPING AND OPTIMIZED GATED CLOCK GENERATION

The flipflops with similar toggling or switching activities are grouped i.e the switching in the inputs must be at the same time instant.In other words switching activity of flipflops are how similarly related to one another.The switching may be either high to low or low to high.The physical synthesis of grouping is described in[12].The sorting of their switching activity[13] is applied.In the group if one of the switching or toggling activity i.e high to low or low to high is similar and the second switching activity is dissimilar,then each flipflop will have different clock pulses at their switching times.The total power consumed by clock includes two parts.

A:Power consumed by the clock pulse at which all flipflops similarly switches.
B:Power consumed by the clock pulses ,where the inputs of the flipflops switches at individual time instants

.

$$P=P_s+P_i \qquad (1)$$

P_s=Power consumed by the flipflops when one switching edge of all the inputs of flipflops is going to happen at same time instant.It is also termed as matching problem[15]

P_i=Power consumed by the flipflops when the other switching edge is going to occur at individual time instants.
Both contributes only to dynamic power dissipation.

The physical position is the second thing to be observed while grouping,otherwise leads to set portioning[16].The obtained outputs are undergone for futher process in the combinational circuits as shown in fig 4

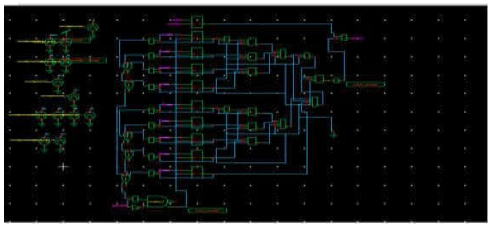

Fig 4.Integrated clockgating for flipflops and their outputs processed in combinational logic in tanner S-edit
In the above figure the values in the combinational circuit will be in the stable state,when the outputs in the flipflops doesnot alter.In such situation leakage current occurs leading to leakage losses.The leakage losses are described in the next section.
Simulation results

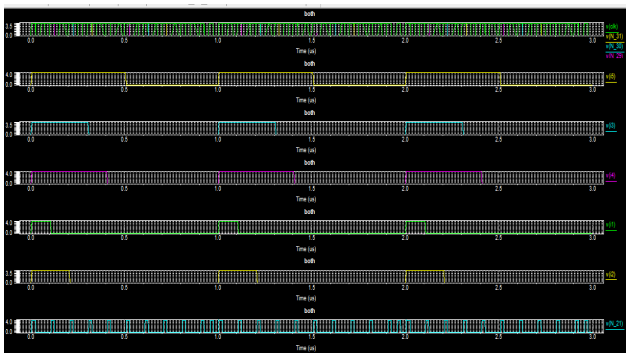

Fig 7 Gated clock signal with first five inputs

The next five inputs with gated clock signal is chown in fig8.The total power consumption in the fig 4 includes dynamic power dissipation and static power dissipation.In the static power dissipation most of the power is consumed by leakage currents,which are eleminated in the successive stages of degisn methodology.

$P_{tot}=P_{dynamic}+P_{static}$ (2)

The circuits are designed in the S-edit of tanner tools TSMC018 CMOS process technology.Each of the circuit of components in the main circuit is converted into blocks of symbol and used. Large dynamic power saving is seen in [18].

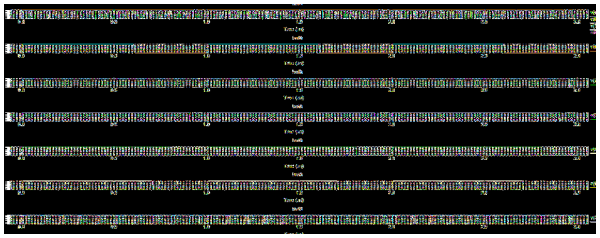

Fig 8 Gated clock signal with next five inputs.

IV PROPOSED INTEGRATION OF POWERGATING

As we are using a nanometer technology there is a chance of flowing currents within the transistor even when the device is off due shortest gate length.Powergating is method is a method of eliminating the leakage currents in combinational circuits.Method involves the inclusion of NMOS transistor in the pull-down section,whose source is connected to ground and drain to the pull-down part of the required circuit ,for which powergating is needed.When there no change of inputs, outputs will not alter,then we can dissconnect the ground for avoiding the flow of leakage currents to ground.This can be achieved by the added NMOS transistor,by switching off the NMOS transistor with giving logic 0 to its gate.The circuit of including Powergating in the existing circuit is shown in fig 9

All the gates present in the combinational circuit are given a common ground.This can be done by considering individual ground of each gate as a port and all these ports are connected to a common point and further common point is connected to single ground as shown in fig 4. As per the process of power gating the common point is connected to drain of NMOS transistor and source of NMOS is connected to ground as shown in fig 9.3-D acceleration[19]and network processor control[17] gives better performance.

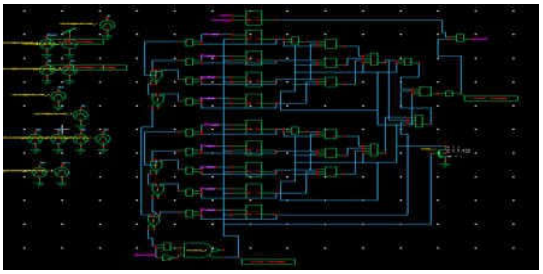

Fig 9 Integration of clock gating and powergating

The controlling of NMOS transistor is achieved from the previous stage of integrated clock gating.The Gated clock signal obtained in the previous stage is added to gate of NMOS transistor as a part of new design.

Powergating can be implemented in two types:fine-grain,in which each gate is individually added a NMOS transistor and coarse grain,where group of gates are combinely applied power gating with common NMOS.

When there is no clock pulse,the combinational circuit is disconnected from ground and no leakage current flows to ground.When the ground is disconnected the in order to preserve the correctness of existing output a latch is included for storing the data otherwise floating occurs in output data.

V. EXPERIMENTAL RESULTS

The comparison of power consumption is done among the three different circuits *A. The normal circuit of without clock gating and power gating,B. Clock gating and without power gating C .Integration of clockgating and power gating* through EDA vendor[20].

Circuit	Power Consumption
Non Clock Gating and Non PowerGating	1.059751×10^{-4} Watts
Clock Gating and Non Power Gating	2.7815×10^{-6} Watts
Integration of Clock Gating and Power Gating	1.698119×10^{-6} Watts
Total Power saved by ClockGating and Power Gating	104.2769×10^{-6} Watts

TABLE 2.COMPARISION OF POWERCONSUMPION

Conclusion

In this Paper, we implemented the Clock gating technique integration in order to reduce the dynamic power in Flip-Flops and later on we implemented the power gating technique in order to reduce leakage power in the combinational circuits. Power in the circuits and their performances are evaluated with sleep technique using Tanner Tools.

Future scope

For Integration of clock gating we must check about the delay produced the clock gating network so in future we can design which can reduce the delay produced by the clock gating circuitry.

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